

AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings of claims in the application.

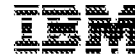
LISTING OF CLAIMS:

What is claimed is:

1 1. (Cancelled)

1 2. (Currently Amended) The circuit for use in a
2 microprocessor, comprising a 4-2 compressor circuit
3 having a full adder formed with a XOR/XNOR cell, said
4 full adder providing a Carry out, a Sum and a
5 complementary sum output signal, according to claim
6 1 wherein the compressor circuit has a full adder
7 circuit and a XOR/XNOR cell and one other instance of
8 said XOR/XNOR cells and two pass-logic 2-1
9 multiplexors, each of said multiplexors being coupled
10 to said full adder and to said one other instance of
said XOR/XNOR cell.

1 3. (Currently Amended) The circuit according to claim
2 2 wherein the 4-2 compressor circuit with a full adder
3 and XOR/XNOR cell is connected by having its three
4 input bits [X, Y and Z] passed into the full adder,
5 which full adder generates said Carry out signal as a
6 first order carry out (Cout), and said intermediate sum
7 (S), and an said intermediate complementary sum (S')
8 and last input bits passed into said one other instance
9 of said XOR/XNOR cell.



1 4. (Currently Amended) The circuit according to claim
2 3 wherein said last input bits (W and Cin) are passed
3 into ~~a second~~ said one other instance of said dual
4 XOR/XNOR cells and generate ~~generating~~ an intermediate
5 XOR signal (I) and an intermediate XNOR signal (I').

1 5. (Currently Amended) The circuit according to claim
2 4 wherein a complementary sum (S') and an intermediate
3 sum (S) are passed into one of the 2-1 MUXs using said
4 intermediate XOR signal (I) as ~~the~~ a control signal and
5 wherein the output of said one of the 2-1 MUXs is (10)
6 the final sum ~~(SUM)~~ (Sum) and said complementary sum
7 (S') and a carry-in bit (Cin) are passed into another
8 of said ~~the final~~ 2-1 MUXs.

1 6. (Original) The circuit according to claim 5 wherein
2 said intermediate XNOR is used as the control signal
3 and a (11) second order carry out (Carry) is generated.